(12) UK Patent Application (19) GB (11) 2 022 953 A

(21) Application No 7920361
(22) Date of filing 12 Jun 1979
(23) Claims filed
12 Jun 1979
18 Sep 1979
(30) Priority data
(31) 53/069793
(32) 12 Jun 1978
(33) Japan (JP)
(43) Application published
19 Dec 1979
(51) INT CL[2]
H03K 5/15
(52) Domestic classification
H3T 1P1 2B2 2B3 2B6
2F1 2G 2T2X 2T3F 3C2 3J
3N 4R 4S 5E HC
G4D CS
(56) Documents cited
GB 2000405A
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GB 1502639
GB 1448122
GB 1444237
GB 1435347
GB 1278373
(58) Field of search
H3T
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(54) Circuit for generating scanning pulses

(57) A circuit for generating scanning pulses has a series of stages, each stage having three insulated gate field effect transistors (MOSTs) T32, T33 and T34. A MOST T31 provides an input ϕ_{IN} to the series of stages. Each stage receives an input 21Z into the gate of the first MOST T32, outputs from the first terminal of the second MOST T33 and synchronizing pulses ϕ_1 are applied to the first MOST T32. One terminal of the third MOST T34 is connected to the earth line Vs, and its gate receives feedback from the second terminal of the second MOST T39 of the next stage but one in the series. A positive pulse applied to the input 21Z appears to have a higher peak at the gate of the first MOST T32 due to the bootstrap capacitances of the first MOST T32. Power consumption is thus small. Other circuit configurations are also disclosed with different arrangements of connections to the three MOSTs.

FIG. 11A

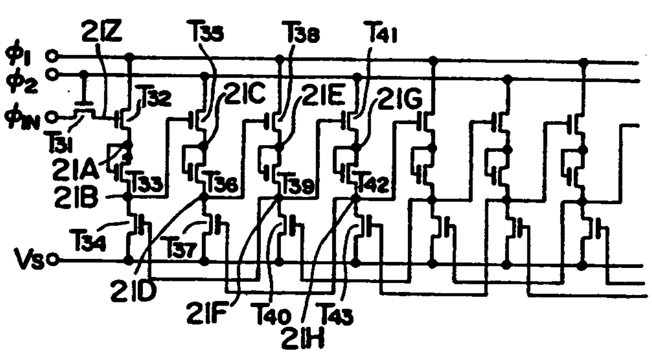

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FIG. 1A

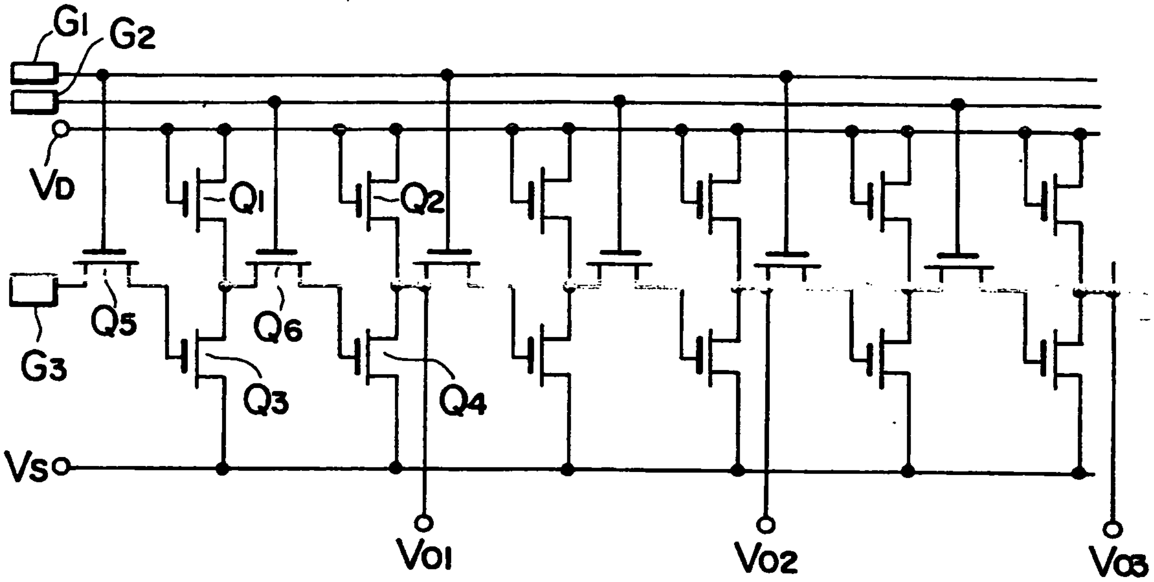

FIG. 1B

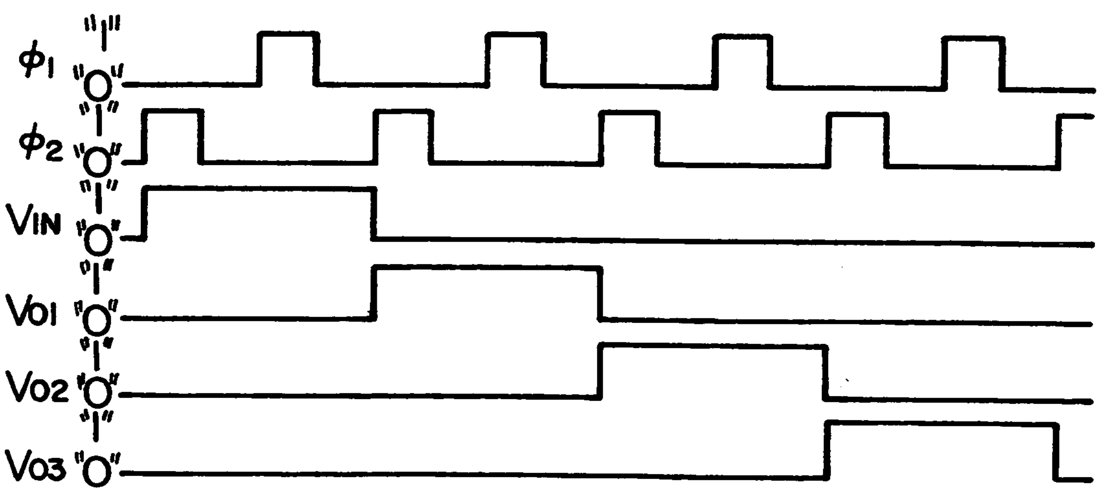

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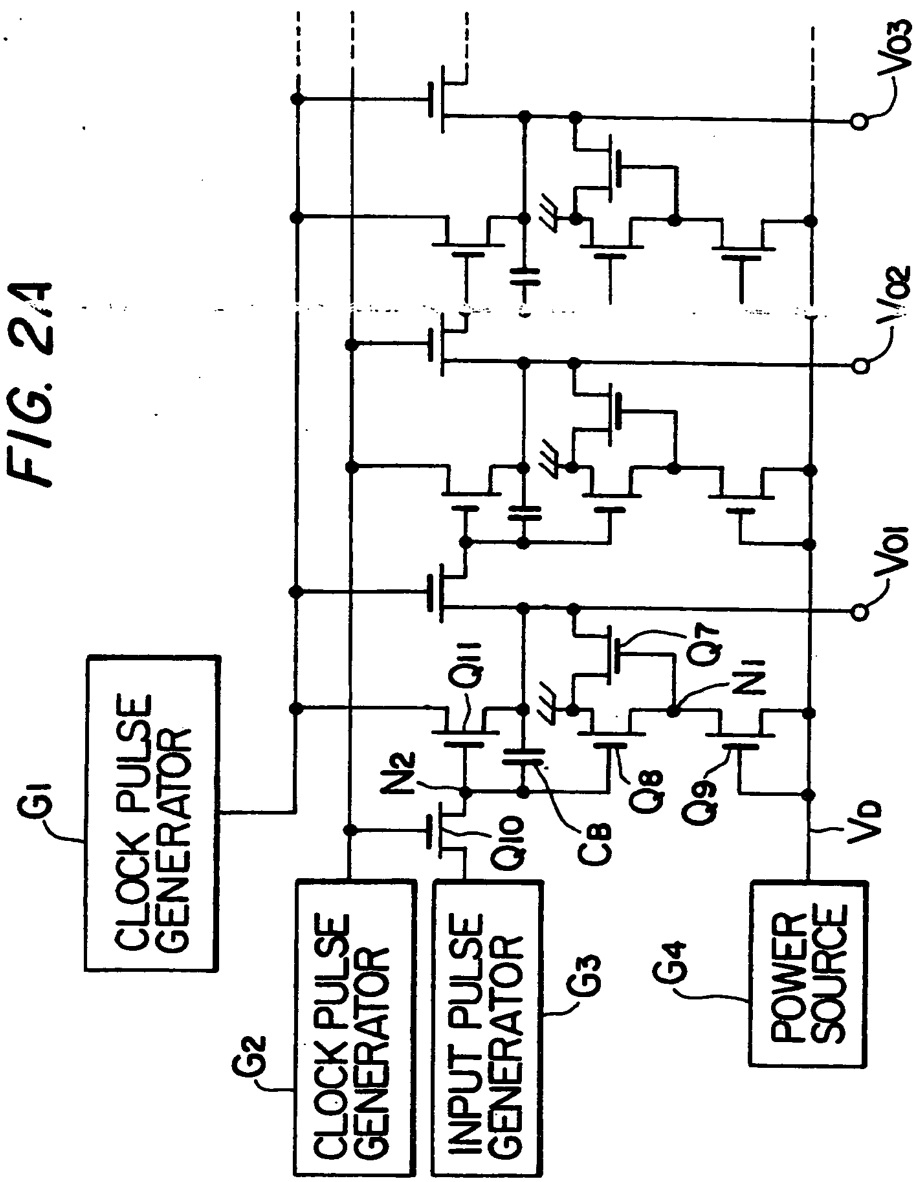
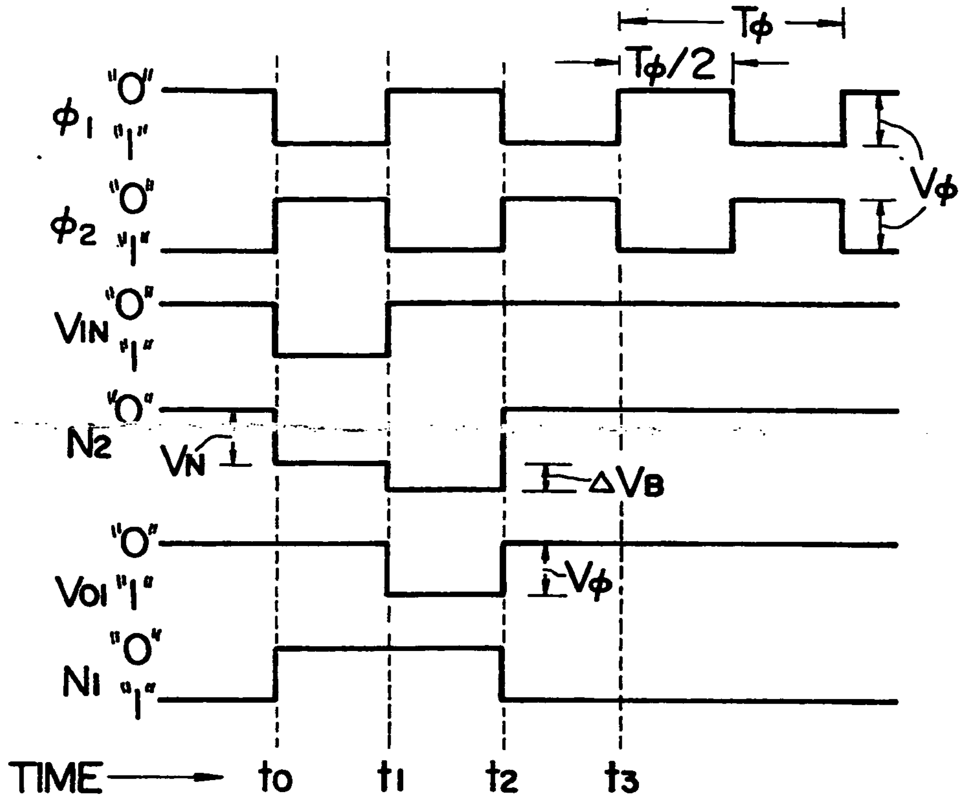
FIG. 2A



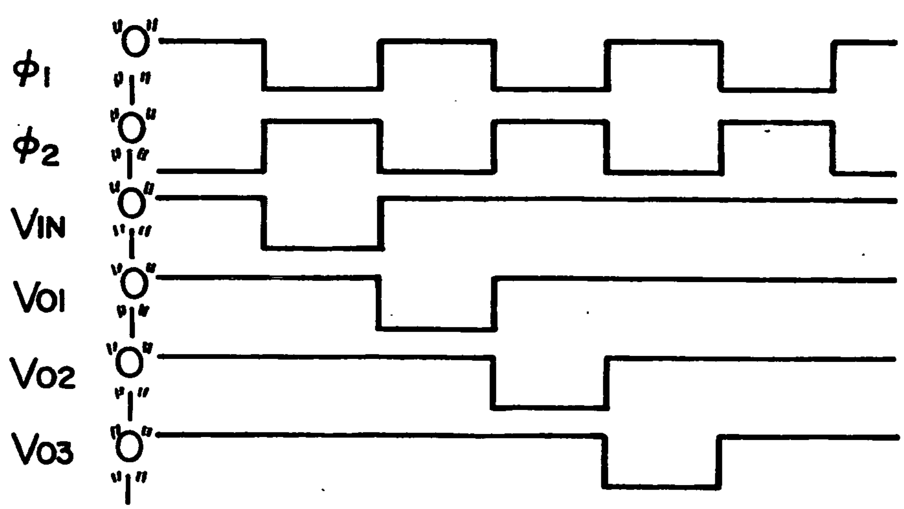
G1
CLOCK PULSE GENERATOR
G2
CLOCK PULSE GENERATOR
G3
INPUT PULSE GENERATOR
G4
POWER SOURCE
Q10
Q11
N2
CB
Q8
Q9
Q7
N1
VD
VO1
VO2
VO3

FIG. 2B



Tφ
Tφ/2
φ1
"0"
"1"
φ2
"0"
"1"
Vφ
VIN
"0"
"1"
N2
"0"
VN
ΔVB
Vo1
"0"
"1"
Vφ
N1
"0"
"1"
TIME
t0
t1
t2
t3

FIG. 2C



φ1
"0"
"1"
φ2
"0"
"1"
VIN
"0"
"1"
Vo1
"0"
"1"
Vo2
"0"
"1"
Vo3
"0"
"1"

FIG. 3A

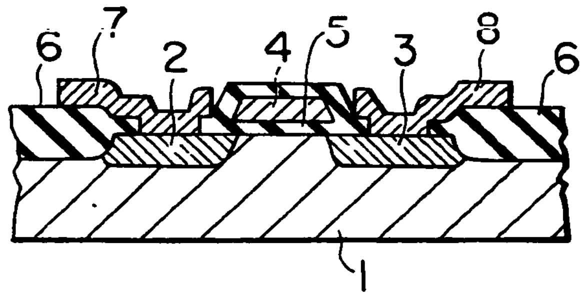


FIG. 3B

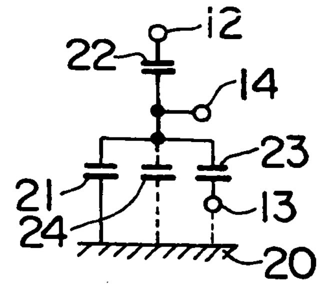


FIG. 3C

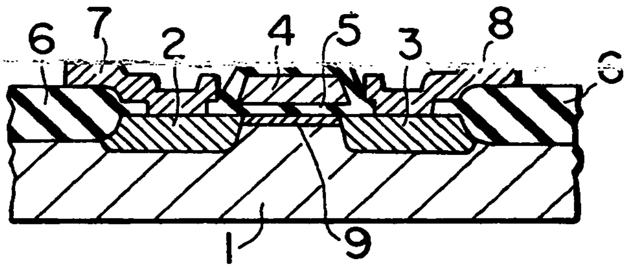


FIG. 3D

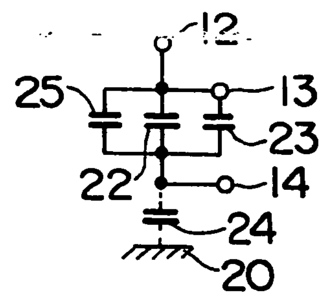


FIG. 4A

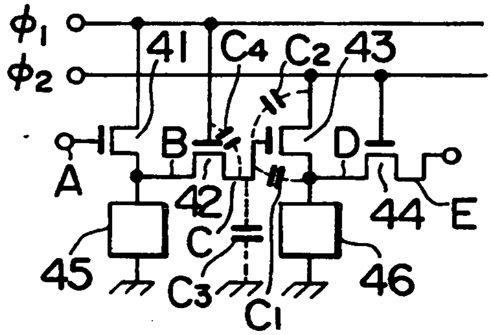


FIG. 4B

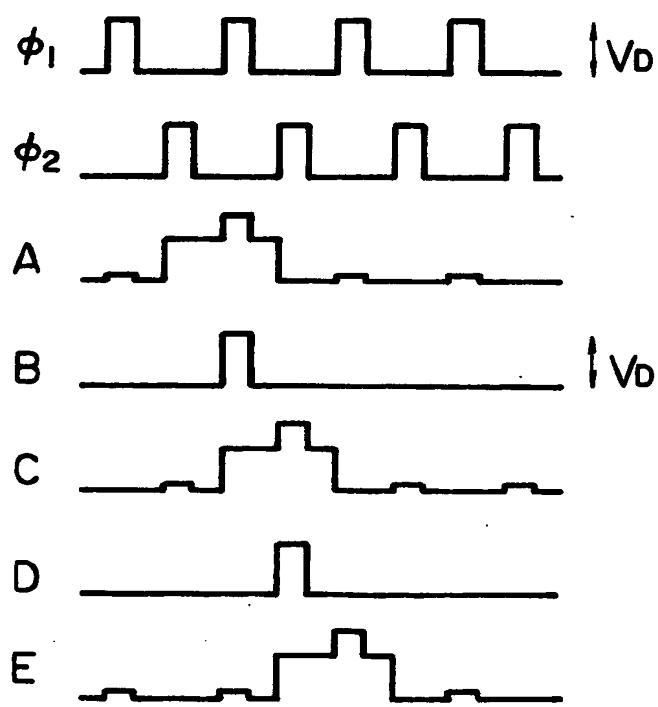


FIG. 5A

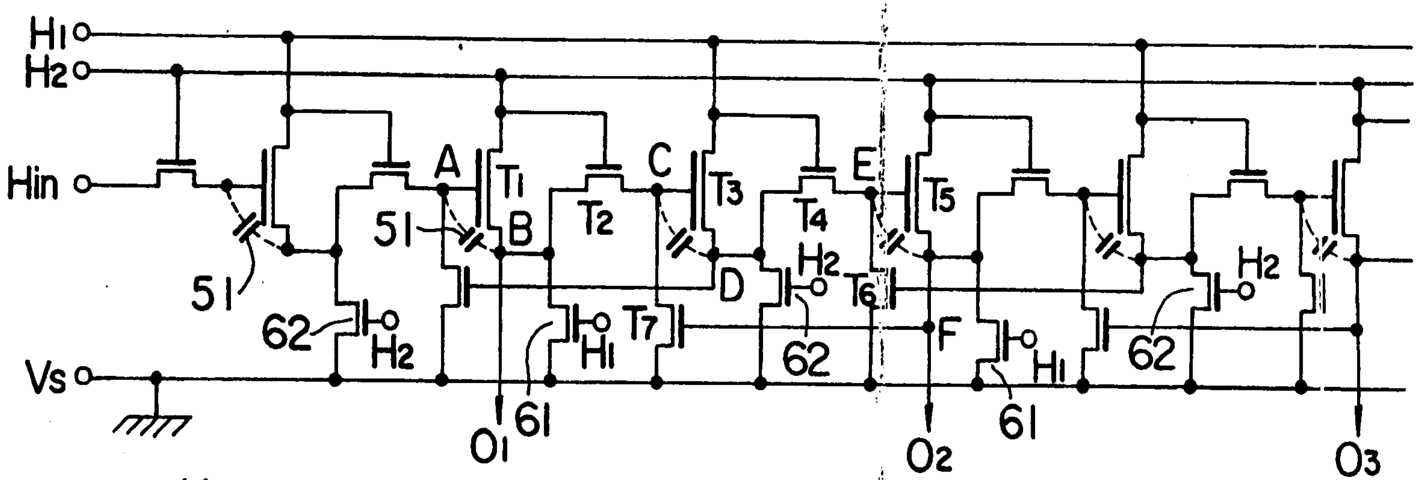
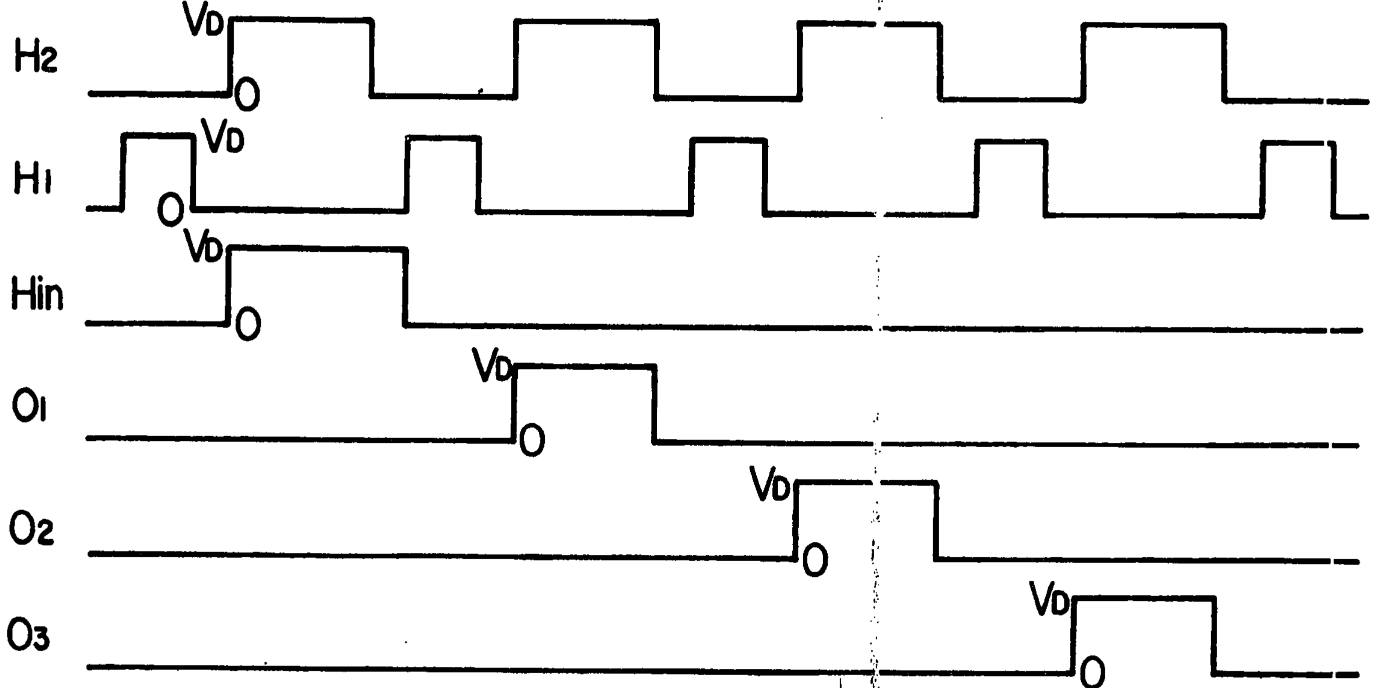

H1
H2
Hin
Vs
A
B
C
D
E
F
T1
T2
T3
T4
T5
T6
T7
51
61
62
O1
O2
O3

FIG. 5B


H2
H1
Hin
O1
O2
O3
VD
0

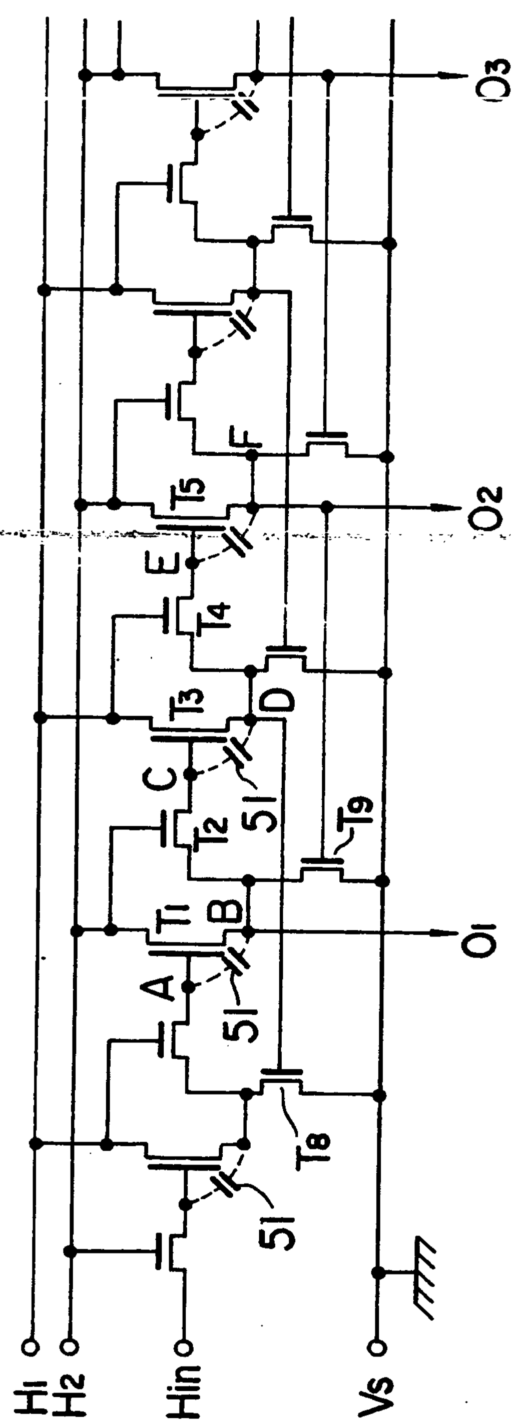

H1
H2
Hin
Vs
O1
O2
O3
A
B
C
D
E
F
T1
T2
T3
T4
T5
T8
T9
51

FIG. 6

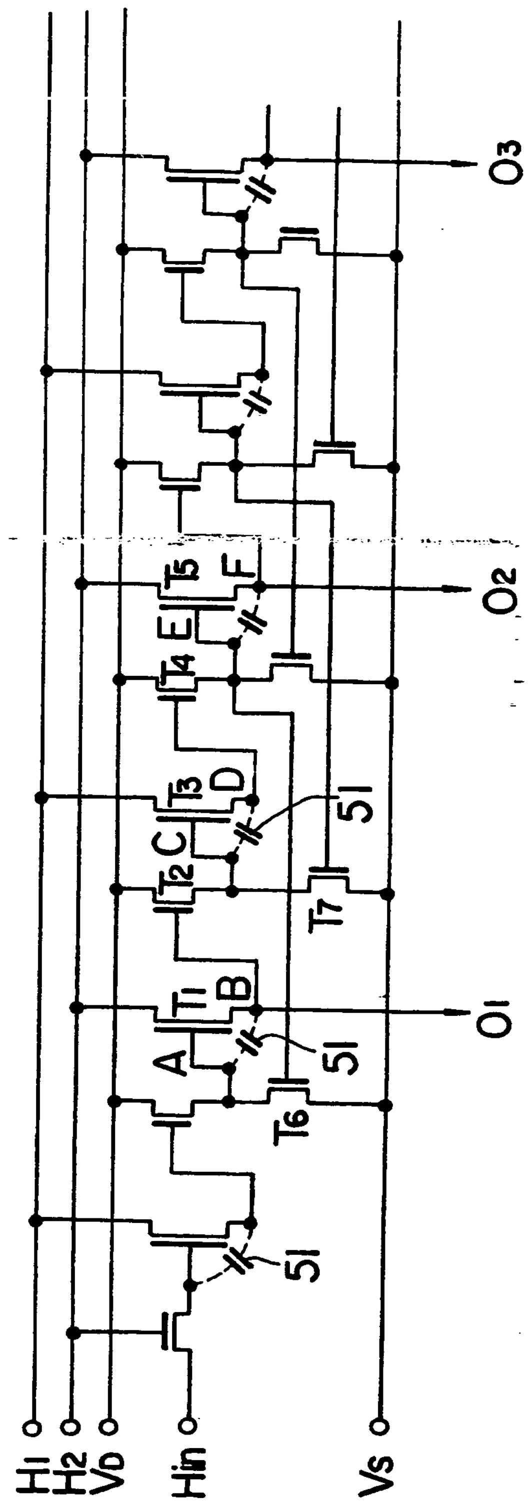

H1
H2
VD
Hin
Vs
O1
O2
O3
A
B
C
D
E
F
T1
T2
T3
T4
T5
T6
T7
51

FIG. 7

FIG. 8

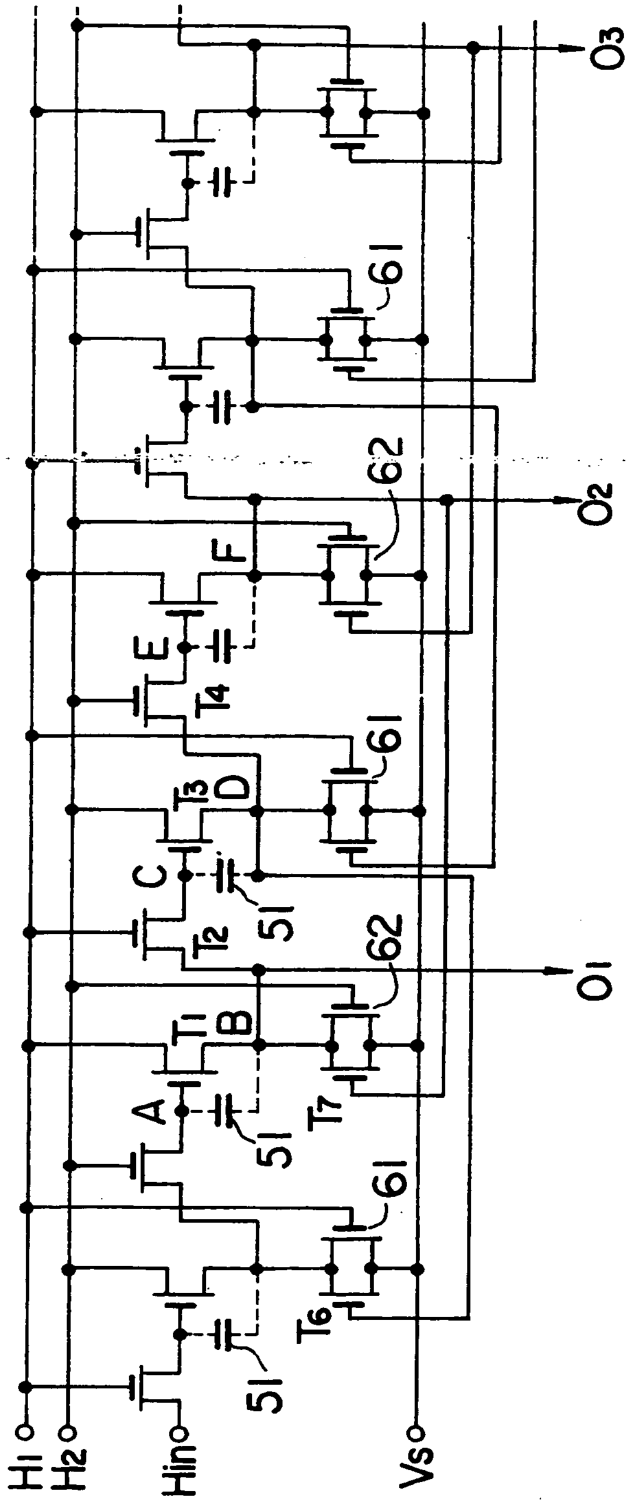


FIG. 9A

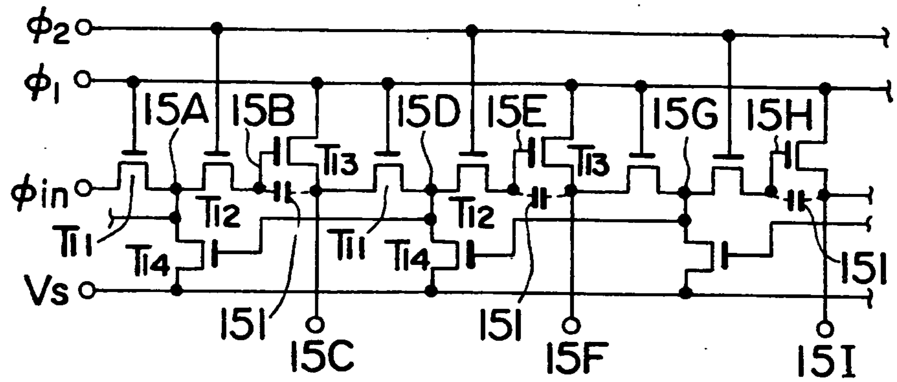

ϕ_2
ϕ_1
ϕin
Vs
15A
15B
15D
15E
15G
15H
T11
T12
T13
T14
151
15C
15F
15I

FIG. 9B

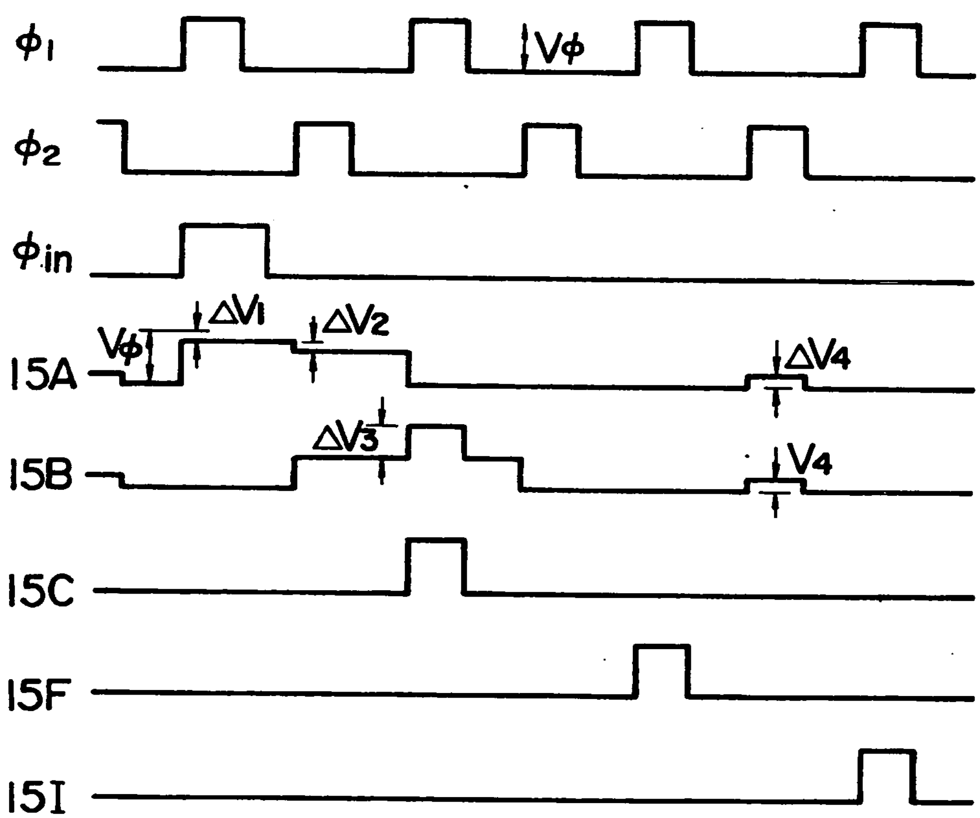

ϕ_1
ϕ_2
ϕin
15A
15B
15C
15F
15I
$V\phi$
ΔV_1
ΔV_2
ΔV_3
ΔV_4
V_4

FIG. 10A

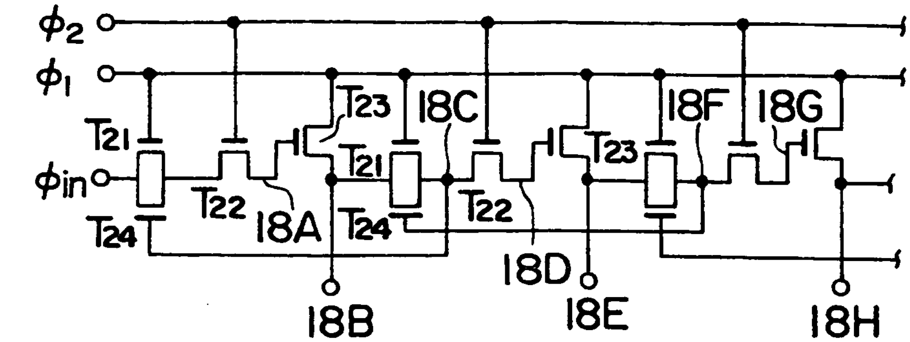


FIG. 10B

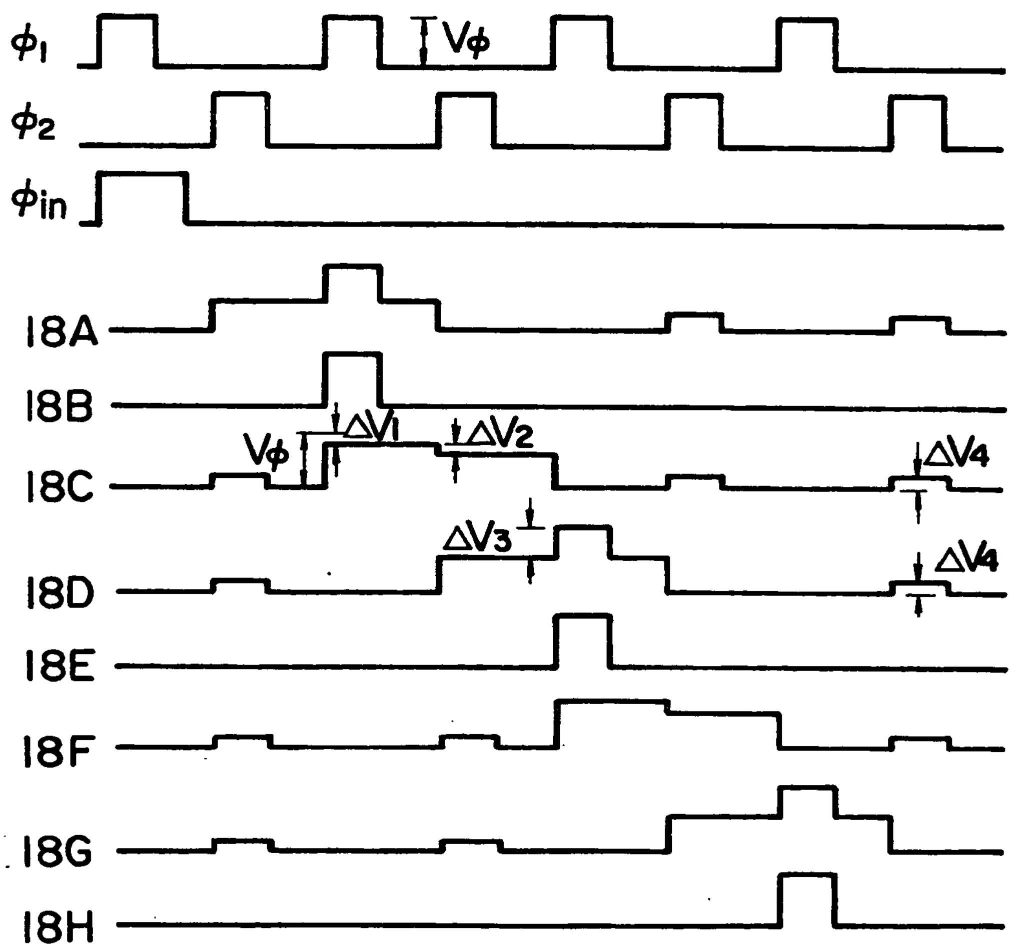


FIG. 11A

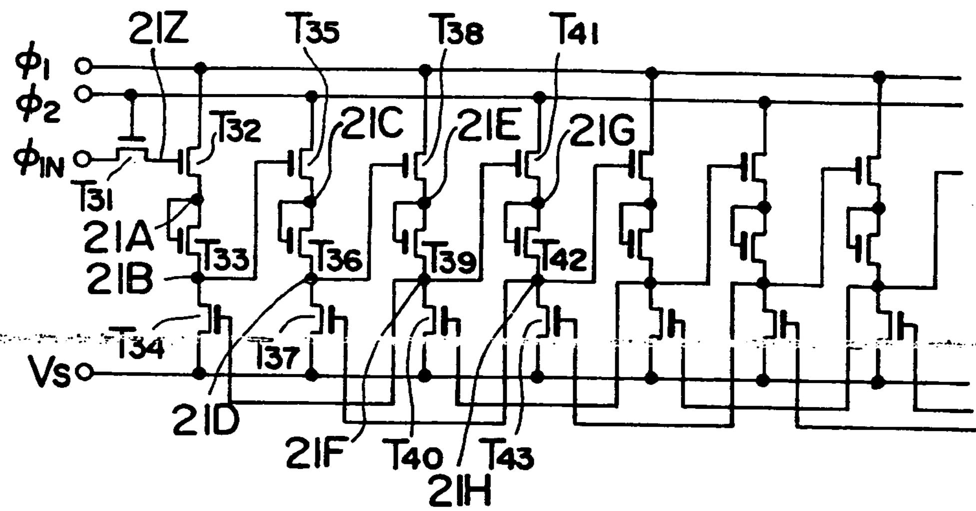


FIG. 11B

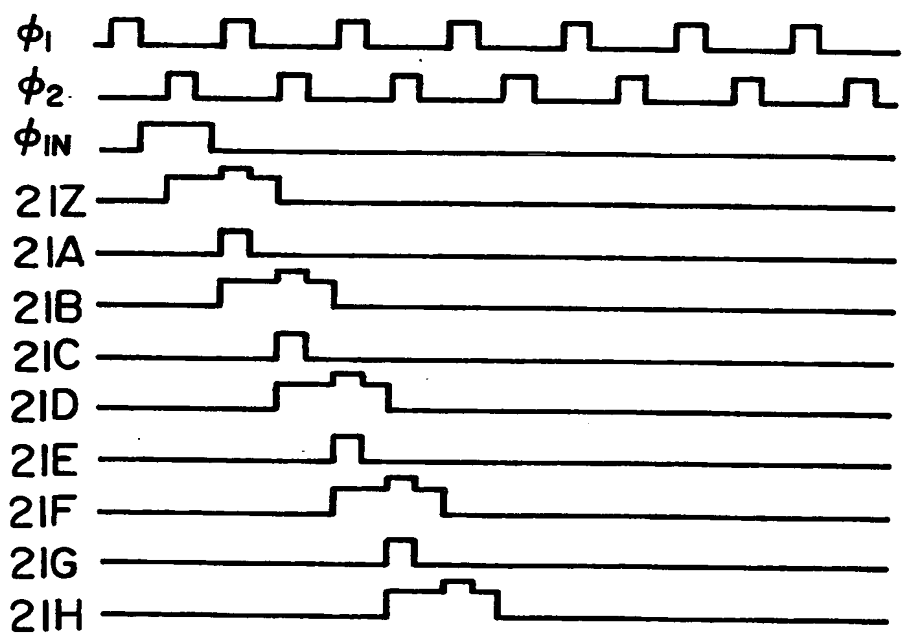


FIG. 12

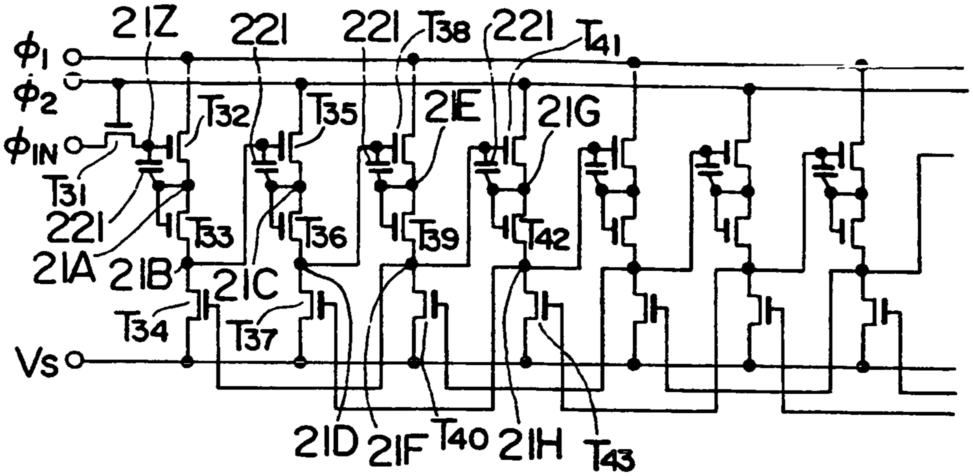


FIG. 13

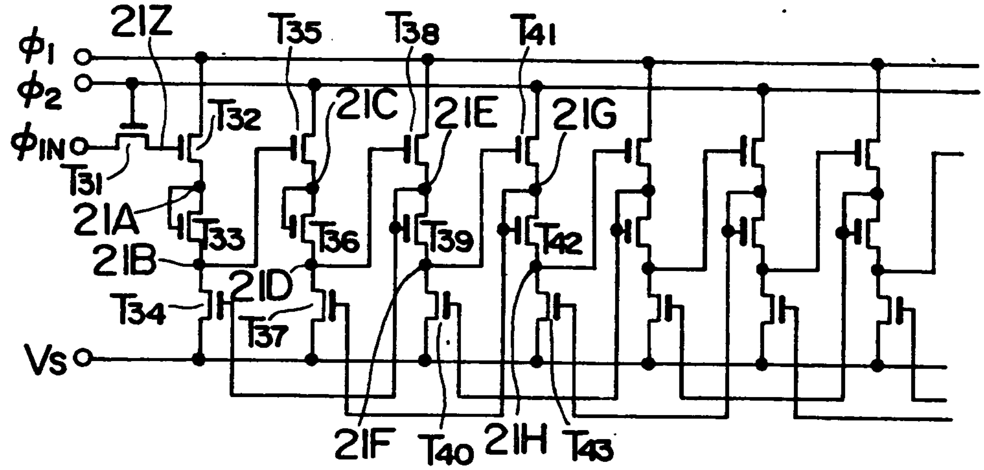


FIG. 14

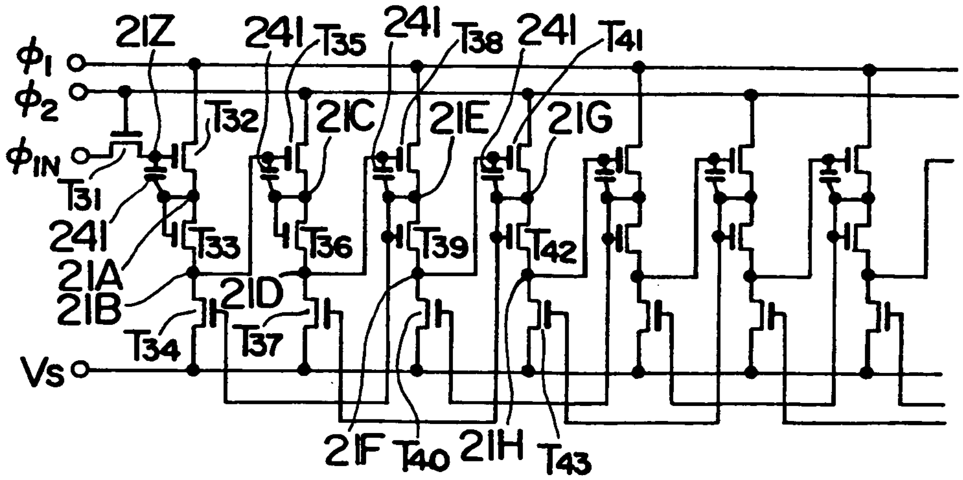
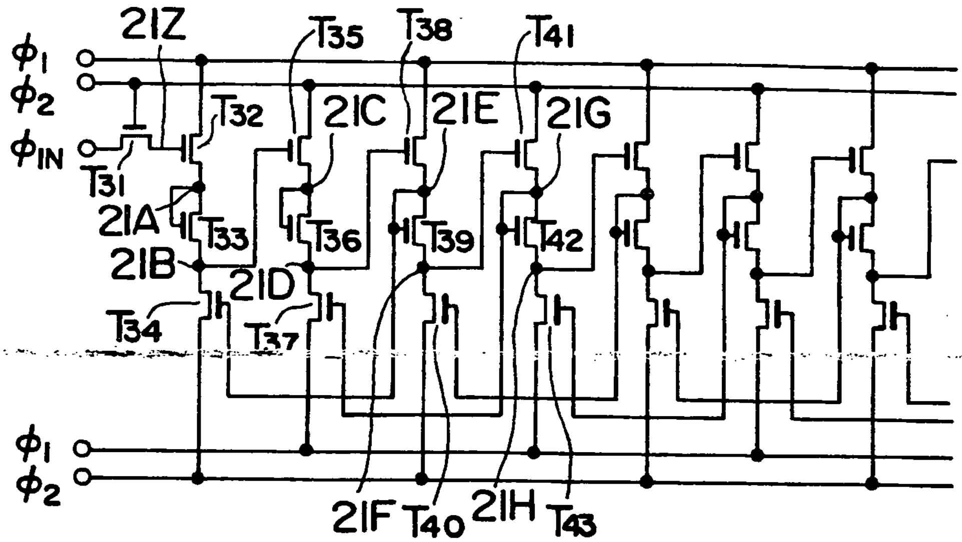
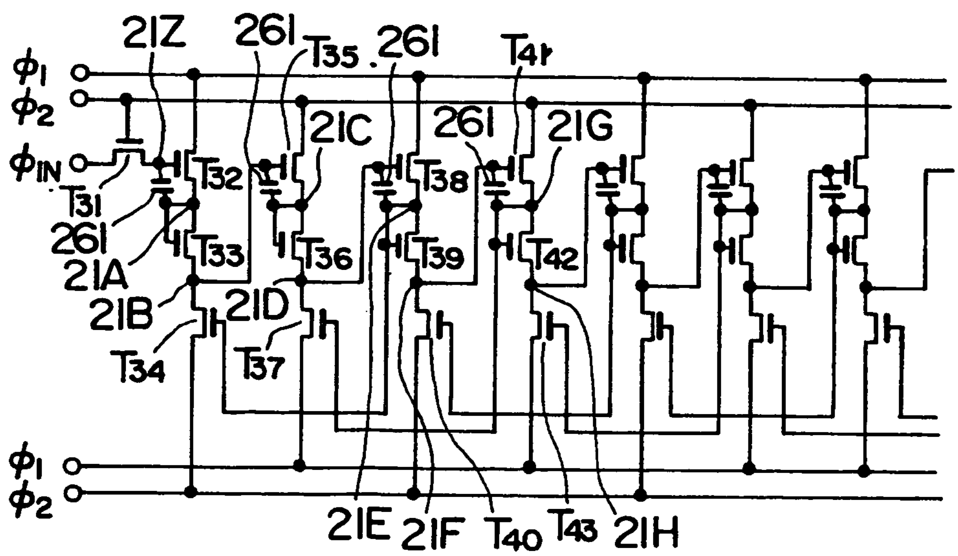


FIG. 15



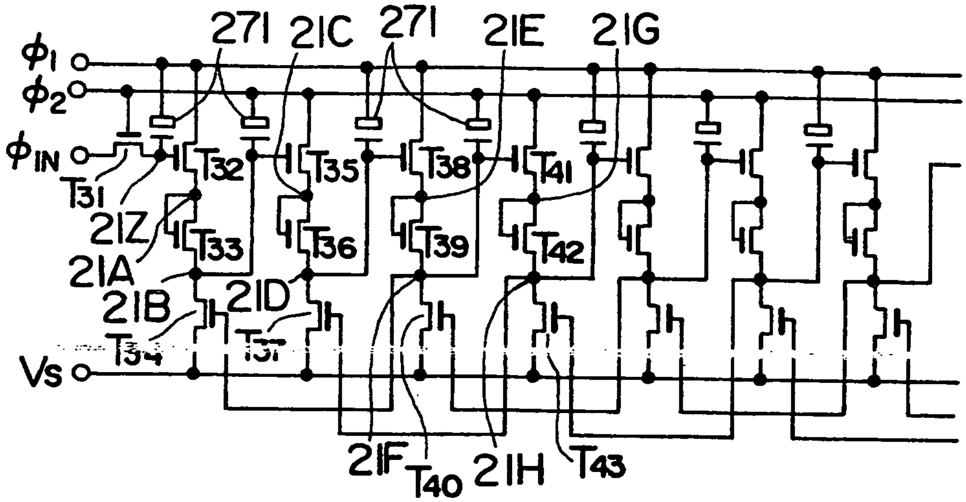
φ1
φ2
φIN
21Z
T35
T38
T41
T32
21C
21E
21G
T31
21A
T33
T36
T39
T42
21B
21D
T34
T37
21F
T40
21H
T43

FIG. 16



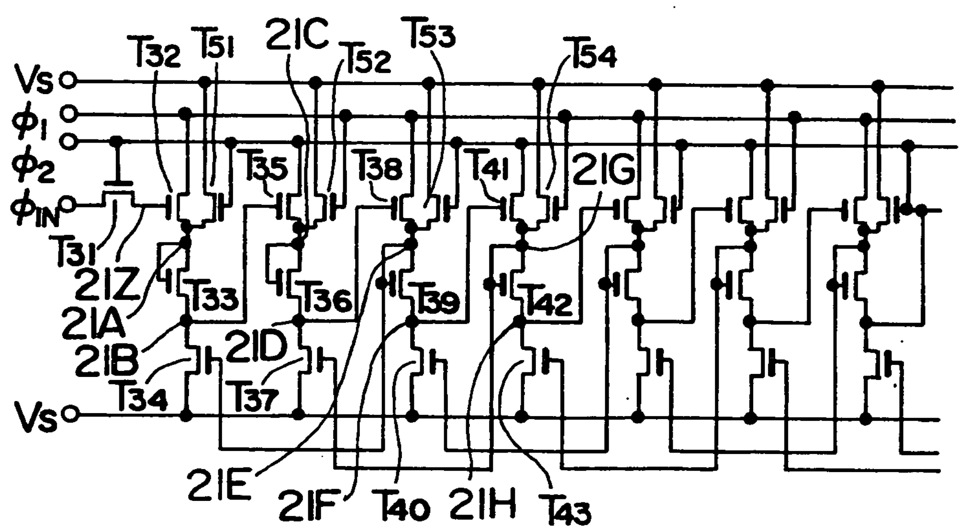
φ1
φ2
φIN
21Z
261
T35
261
T41
21C
261
21G
T32
T38
T31
261
21A
T33
T36
T39
T42
21B
21D
T34
T37
21E
21F
T40
T43
21H

FIG. 17



φ1
φ2
φIN
Vs
271
21C
271
21E
21G
T31
21Z
21A
21B
T34
T32
T33
T35
T36
21D
T37
T38
T39
T41
T42
21F
T40
21H
T43

FIG. 18



Vs
φ1
φ2
φIN
Vs
T32
T51
21C
T52
T53
T54
T35
T38
T41
21G
T31
21Z
21A
21B
T34
T33
T36
21D
T37
T39
T42
21E
21F
T40
21H
T43

14

FIG. 19A

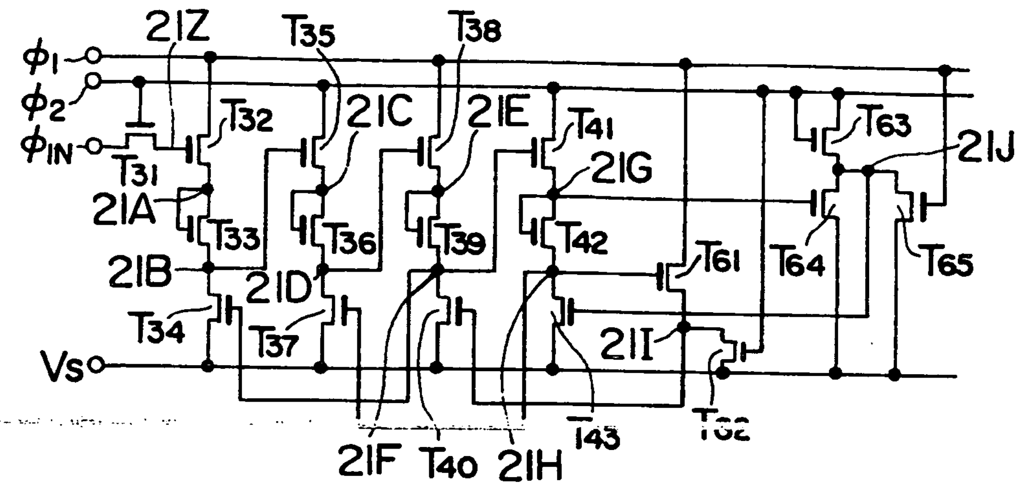
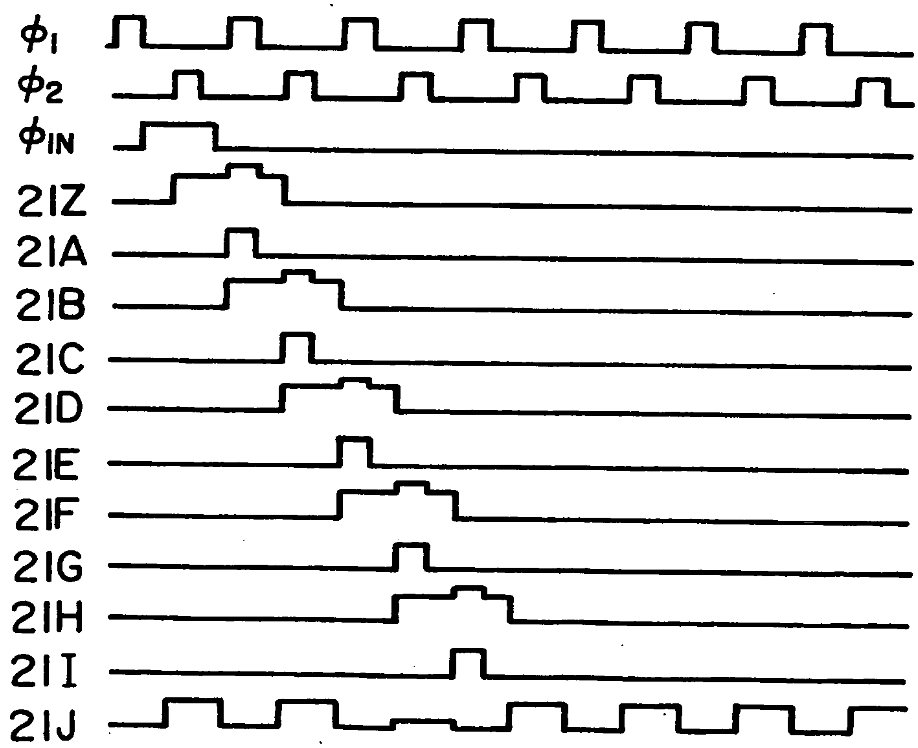


FIG. 19B



SPECIFICATION

Circuit for generating scanning pulses

The present invention relates to a circuit for generating scanning pulses, and more particularly to a circuit for generating scanning pulses which is constructed from a semiconductor integrated circuit. Further, the present invention relates to a pulse generator which generates pulses for selectively scanning sequentially and digitally, a large number of photoelectric conversion elements situated in an optical reader, or a photosensor array of a facsimile, or a solid-state imager, especially to such scanning pulse generator which is constructed of an integrated circuit composed of MIS (Metal-Insulator-Semiconductor) insulated gate field-effect transistors.

It is known in the prior art that a circuit for generating scanning pulses may use a shift register type scanning circuit wherein, in order to sequentially scan a large number of photoelectric conversion elements in a linear or coplanar arrangement, input pulses are delayed for a fixed time and then delivered in succession by the use of two or more phases of synchronizing pulses as illustrated in Figure 1A of the accompanying drawings. This figure shows a circuit diagram of the first three stages of the shift register type scanning circuit employing Metal-Insulator-Semiconductor insulated gate field-effect transistors hereinafter referred to as "MISTs").

Generators G_1 and G_2 generate synchronizing pulses ϕ_1 and ϕ_2 respectively, and a generator G_3 produces pulses V_{IN}. Also shown is a D.C. power supply V_D, and a reference voltage terminal V_S which usually is earthed. Transistors Q_1 and Q_2 are load MISTs which are in the saturation state because the gate and drain electrodes thereof are converted to the power supply V_D. Transistors Q_3 and Q_4 are driver MISTs. A circuit in which the source electrode of the MIST Q_1 and the drain electrode of the MIST Q_3, or the source electrode of the MIST Q_2 and the drain electrode of the MIST Q_4 are combined in series operates as an inverter. Transistors Q_5 and Q_6 are transfer MISTs.

Although the following description will be made by taking N-channel MISTs as an example and employing a positive logic system (in which a positive high voltage is expressed by "1" and the earth voltage by "0"), the description also applies to P-channel MISTs by inverting the signs of the voltages. The input pulse V_{IN} which is applied to the first stage inverter by the input pulse generator G_3 is delayed by a fixed time determined by the synchronizing pulses ϕ_1 and ϕ_2, during the passage through each stage, by the transfer MISTs which are alternately turned "on" and "off" by the synchronizing pulses ϕ_1 and ϕ_2. The delayed pulses appear at output terminals V_{01}, V_{02} and V_{03} of the respective stages as illustrated in the waveform diagram shown in Figure 1B of the accompanying drawings.

The shift register type scanning circuit utilizing the MISTs is suited to a semiconductor integrated circuit in that all the circuit elements can be fabricated from the MISTs and that the fabrication process is comparatively simple. The density of elements on the integrated circuit and the available percentage are also enhanced. Since the operating margin is high and the deviations of the characteristics of the respective stages are small, the foregoing scanning circuit is excellent for use as a scanning circuit which requires many output stages.

The scanning circuit described above, however, has the following disadvantages:

(a) Current flows through one of the two stages of inverters at all times, so that the power dissipation is high.

(b) Notwithstanding that the ability to power a load is determined by the MIST Q_2 (or Q_1), the channel width of the driver transistor MIST Q_4 (or Q_3) depending on the size of the transistor) must be made large, so that a large area is occupied by these circuit elements in an integrated circuit. More specifically, the output offset voltage V is given by the equation:

$$V = V_D \times \frac{g_m(Q_2)}{g_m(Q_4)} \approx V_D \frac{L_2}{L_4}$$

where

V_D: supply voltage,
$g_m(Q_2)$: conductance of MIST Q_2,
$g_m(Q_4)$: conductance of MIST Q_4,
L_2: channel width of MIST Q_2,
L_4: channel width of MIST Q_4.

In order to make the offset small, the channel width L_4 of the MIST Q_4 must be made large, so that the area of the MIST Q_4 increases.

(c) The variation of outut signal voltage is small compared with the supply voltage. The "0" level of the output does not reach earth potential (it becomes approximately $V_D \cdot g_m(Q_2)/g_m(Q_4)$), and the "1" level of the output does not reach the potential of the power supply, either.

(d) The deviation of the threshold voltage of the MIST Q_4 has great influence on the behaviour of the circuit.

In addition to the scanning circuit shown in Figure 1A, a shift register constructed of complementary MISTs (CMOS) has been devised. Using a CMOS circuit, the operating speed is high and the power dissipation is low, and the number of constituent elements per stage decreases. However, N-channel MISTs and P-channel MISTs must be integrated, and the manufacturing process becomes complicated. It is therefore desirable to construct the scanning circuit by the use of MISTs with the same type of channel.

Another type of scanning circuit is known which exploits the bootstrap effect of MISTs. Figure 2A of the accompanying drawings shows the scanning circuit exploiting the bootstrap effect as proposed by N. Koike and disclosed in U.S. Patent Application Serial No. 764,841 and German Offenlegungsschrift No. 27.05,429).

In Figure 2A, a MIST Q_{10} serves to transfer an input pulse (level "1" or "0") supplied from an input pulse generator G_3, under the control of a synchronizing pulse; a charging MIST Q_{11} is connected on the output side of the transfer MIST Q_{10} and serves to deliver a scanning output pulse to an output side terminal V_{01} under the control of another synchronizing pulse; and discharging MIST Q_7 is connected between the output side of the charging MIST Q_{11} and an earth line and which serves to discharge charges stored in an output terminal circuit.

Also, a driving MIST Q_8 and a load MIST Q_9 are connected in cascade between a power supply line V_D and the earth line, and the gate electrode of the discharging MIST Q_7 is connected to the junction N_1 between both the MISTs Q_8 and Q_9. The junction N_2 between the transfer MIST Q_{10} and the charging MIST Q_{11} is connected to the gate electrode of the driving MIST Q_8. A bootstrap capacitance GB is connected between the source and gate electrode of the charging MIST Q_{11}.

Figure 2B of the accompanying drawings, shows the waveforms of the synchronizing pulses ϕ_1 and ϕ_2, the input pulse V_{IN} and pulses at the junction N_2, the output terminal V_{01} and the junction N_1.

The scanning circuit of Figure 2A is such that a unit circuit is made up of five MISTs Q_7, Q_8, Q_9, Q_{10} and Q_{11}, and the basic circuits are connected in many stages. Figure 2C of the accompanying drawings shows a waveform diagram of the synchronizing pulse ϕ_1 and ϕ_2, the input pulse V_{IN} and output pulses V_{01}, V_{02} and V_{03}.

This scanning circuit exploiting the bootstrap effect of MISTs has the advantage that it is no longer necessary to provide a continuous current to hold the stage of an inverter, so the power dissipation is reduced. However, it has the disadvantage that noise in the bandwidth is likely to occur due to the difference of the waveforms of the synchronizing pulses ϕ_1 and ϕ_2 (due to the difference between the pulse shaping units). The scanning circuit of Figure 2A requires the five MISTs and one bootstrap capacitance of sufficiently large capacitance to form the fundamental constituent elements for each stage and has not got a simple construction so that a problem remains due to the density of elements on the integrated circuit.

A scanning circuit exploiting the bootstrap effect has also been disclosed in U.S. Patent Specification No. 3,829,711. It also required five MISTs, forming constituent elements of each stage, which forms a problem due to the density of elements in the integrated circuit.

According to a first aspect of the present invention there is provided a circuit for generating scanning pulses comprising a plurality of stages of basic circuits connected in series, each basic circuit including a first a second and a third insulated gate field-effect transistors (hereinafter referred to as MISTs), each MIST having a first and a second terminal and a gate terminal;

the first terminal of said first MIST being used as a synchronizing-pulse-applying terminal, the second terminal of said first MIST being used as a scanning pulse output terminal, and the gate terminal of said first MIST being used as an input terminal;

the first terminal and the gate terminal of said second MIST being electrically connected together and to the second terminal of said first MIST, and the second terminal of said second MIST being used as an output terminal;

the first terminal of said third MIST being electrically connected to the second terminal of said second MIST, the second terminal of said third MIST being used as an earth terminal, and the gate terminal of said third MIST being used as a feedback input terminal.

According to a second aspect of the present invention there is provided a circuit for generating scanning pulses comprising a plurality of stages of basic circuits connected in series, each basic circuit including a first a second and a third insulated gate field-effect transistors (hereinafter referred to as MISTs), each MIST having a first and a second terminal and a gate terminal;

the first terminal of said first MIST being used as a synchronizing-pulse-applying terminal, the second terminal of said first MIST being used as a scanning pulse output terminal, and the gate terminal of said first MIST being used as an input terminal;

the first terminal of said second MIST being electrically connected to the second terminal of said first MIST, the second terminal of said second MIST being used as an output terminal, and the gate terminal of said second MIST being connected to the synchronizing-pulse-applying terminal;

the first terminal of said third MIST being electrically connected to either the scanning pulse output terminal or the output terminal, the second terminal of said third MIST being used as an earth terminal, and the gate terminal of said third MIST being used as a feedback input terminal.

According to a third aspect of the present invention there is provided a circuit for generating scanning pulses comprising a plurality of stages of basic circuits connected in series, each basis circuit including a first a second and a third insulated gate field-effect transistors (hereinafter referred to as MISTs), each MIST having a first and second terminal and a gate terminal;

the first terminal of said first MIST being used as a synchronizing-pulse-applying terminal, the second terminal of said first MIST being used as a scanning pulse output terminal, and the gate terminal of said first MIST being used as an input terminal;

the first terminal of said second MIST being used as a power supply terminal, the second terminal of said second MIST being used as an output terminal, and the gate terminal of said second MIST being electrically connected to the second terminal of said first MIST

the first terminal of said third MIST being electrically connected to either the scanning pulse

output terminal or the output terminal, the second terminal of said third MIST being used as an earth terminal, and the gate terminal of said third MIST being used as a feedback input terminal.

The present invention will now be described in greater detail, by way of example, with reference to the remaining figures of the accompanying drawings, wherein:—

Figures 3A and 3C are schematic sectional views through Metal Oxide — Semiconductor insulated gate field-effect transistors (hereinafter referred to as MOSTs);

Figures 3B and 3D are circuit diagrams showing parasitic capacitances of the MOSTs;

Figure 4A is a circuit diagram showing a circuit for generating scanning pulses which utilizes the bootstrap effect of MISTs;

Figure 4B is a waveform diagram showing potential changes at various nodes in the circuit shown in Figure 4A;

Figure 5A is a circuit diagram showing a first embodiment of a scanning pulse generator circuit according to the present invention;

Figure 5B is a waveform diagram showing synchronizing pulses, an input pulse and output pulses in the circuit shown in Figure 5A;

Figure 6 is a circuit diagram showing a modification of the circuit shown in Figure 5A;

Figure 7 is a circuit diagram showing a second embodiment of the scanning pulse generator circuit according to the present invention;

Figure 8 is a circuit diagram showing a third embodiment of the scanning pulse generator circuit according to the present invention;

Figure 9A is a circuit diagram showing a fourth embodiment of the scanning pulse generator circuit according to the present invention;

Figure 9B is a waveform diagram showing synchronizing pulses, an input pulse and potential changes at various points in the circuit shown in Figure 9A;

Figure 10A is a circuit diagram showing a fifth embodiment of the scanning pulse generator circuit according to the present invention;

Figure 10B is a waveform diagram showing synchronizing pulses, an input pulse and potential changes at various points in the circuit shown in Figure 10A;

Figure 11A is a circuit diagram showing a sixth embodiment of the scanning pulse generator circuit according to the present invention;

Figure 11B is a waveform diagram showing synchronizing pulses, an input pulse and potential changes at various points in the circuit shown in Figure 11A;

Figures 12 to 18 are circuit diagrams each showing a modification of the scanning pulse generator circuit shown in Figure 11A;

Figure 19A is a circuit diagram showing a terminating circuit of the scanning pulse generator circuit shown in Figure 11A; and

Figure 19B is a waveform diagram showing synchronizing pulses, an input pulse and potential changes at various points in the circuit shown in Figure 19A.

The present invention consists of a semiconductor device in which a dynamic scanner (shift register) is constructed by exploiting the bootstrap effect of MISTs.

The bootstrap effect exploited in the scanning pulse generator circuit of this invention will now be described with reference to an N-channel MOST in which signal charges are electrons and which employs an SiO_2 film as a gate insulating film. In Figures 3A and 3C is shown a silicon substrate 1 of P-type conductivity, N-type diffused layers 2 and 3 to serve as a drain electrode and a source electrode respectively, a gate electrode 4 a gate insulating film 5 (for example, made of SiO_2), a field oxide film 6 (for example made of SiO_2), drain and source electrode connections 7 and 8 respectively, and an N-type inversion layer 9. In Figure 3A, when the gate electrode 4 is at zero Volts, no inversion layer is formed in the surface of the P-type Si substrate 1 underlying the gate oxide film 5. When a positive voltage (of a voltage greater than the threshold voltage V_{th} of the MOST) is applied to the gate electrode 4, the N-type inversion layer 9 is formed as illustrated in Figure 3C, and the N-type diffused layers 2 and 3 are electrically connected. By way of example, the capacitive coupling between the N-type diffused layer 2 and the gate electrode 4 is illustrated in Figures 3B and 3D.

When the gate electrode 4 is at zero volts, the coupling capacitance between a terminal 12 corresponding to the N-type diffused layer 2 and a terminal 14 corresponding to the gate electrode 4 consists only of a capacitance 22 due to their structural overlap. The terminal 14 has an overlap capacitance 21 between the gate electrode 4 substantially connected to earth 20 and P-type Si substrate 1, an overlap capacitance 23 between the gate electrode 4 and the N-type diffused layer 3 indicated by a terminal 13, which form parasitic capacitances which suppress the effect of the coupling capacitance 22 and a parasitic capacitance 24 of the other parts connected to the gate electrode 4 (Figure 3B).

Alternatively, in the case where the positive voltage ($>V_{th}$) is applied to the gate electrode 4, the capacitive coupling between the gate electrode 4 (terminal 14) and the N-type diffused layer 2 (terminal 12) includes, in addition to the capacitance 22, the sum of a capacitance 25 between the gate electrode 4 and the inversion layer 9 to replace the capacitance 21 and the overlap capacitance 23 between the gate electrode 4 and the N-type diffused layer 3 (terminal 13). It is only the parasitic capacitance 24 that is connected to earth 20. The capacitances 22 and 23 are usually equivalent. The capacitances 21 and 25 are also substantially equal, and ordinarily they have a value nearly one order greater than the capacitance 22.

Hence, the junction capacitance between the N-type diffused layer 2 and the gate electrode 4 has the nature of a varactor capacitance which varies greatly depending upon the voltage applied to the gate electrode 4. It produces the bootstrap-

like effect that when a positive voltage is applied to the gate electrode 4 in advance, the impression of a positive pulse on the N-type diffused layer 2 raises further the voltage of the gate electrode 4.

The present invention consists of a circuit for generating scanning pulses which utilizes the property of the varactor capacitance, and this principle is illustrated in Figures 4A and 4B. Figure 4A shows two stages which correspond to a basic circuit, whilst Figure 4B shows a waveform diagram of principal points A to E. Loads 45 and 46 may be resistances, capacitances or a combination thereof. When, in the case where the voltage of the point C is made positive in advance, a synchronizing pulse ϕ_2 becomes positive, the potential of the point C is raised and a MOST 43 applies the synchronizing pulse ϕ_2 to the load 46 under a non-saturation condition.

Design conditions may fulfill the following. Assuming, by way of example, that the voltage drop of the point C at the time when the point B has become positive is ΔV (= $V_{th} + K\sqrt{V_D - V_{th}}$; where V_D is the amplitude of ϕ_1 and ϕ_2, and K is the body effect constant), the following equations hold.

$$\frac{(C_1 + C_2)V_D}{C_1 + C_2 + C_3 + C_4} \geq \Delta V \quad \ldots\ldots\ldots (1)$$

$$\frac{C_2 V_D}{C_1 + C_2 + C_3 + C_4} \leq V_{th} \quad \ldots\ldots\ldots (2)$$

In the case where the loads 45 and 46 have a low value of resistance of capacitance, a capacitance or high resistance (of the order of 10^5 to 10^7 ohms in ordinary IC element dimensions and uses) is connected in parallel therewith or a MOST which can cause a small amount of current to flow steadily or intermittently by applying a D.C. voltage or intermittent voltage to its gate electrode is situated in parallel therewith, and it may then be considered to be part of the load.

The scanning pulse generator circuit of the present invention utilizes the bootstrap effect, and is therefore very simple in construction. It does not require the driver MOST being disproportionately large in comparison with the load as in the conventional inverter, and it is suited to being fabricated from an integrated circuit. It has a low power dissipation. In addition, since the applied pulses ϕ_1 and ϕ_2 are applied to the loads unchanged the fluctuations of the pulses to be applied to the loads, due to the deviations of the characteristics of the MOSTs constituting the generator circuit, (for example, the deviations of the threshold voltages V_{th}), do not occur, and the lowering of the amplitude does not occur. Particularly in the case where the scanning pulse generator circuit is applied to analog devices, (for example, an image device such as solid-state imager and frame memory) noise can be substantially reduced. When compared with the prior-art circuit for generating scanning pulses which utilizes the bootstrap effect, the circuit for generating scanning pulses according to the present invention can reduce the number of constituent elements and reduce the development of noise. Further, the potentials of the various points in the circuit can be easily reset to zero.

The present invention will now be described in detail with reference to a series of embodiments.

The circuit shown in Figure 5A is a first embodiment of the scanning pulse generator circuit according to the present invention. In Figure 5B, are synchronizing pulses H_1 and H_2, an input pulse H_{in}, and output pulses O_1, O_2 and O_3, with which, for example, switching MIS transistors for horizontal scanning in a solid-state imager are switched.

Referring to Figure 5A, it is now supposed that a point A is at a high level (hereinafter abbreviated to "H"). When the synchronizing pulse H_2 is subsequently applied (it becomes "H"), the potential of a point B rises through a MOST T_1. The potential of the point A rises above a pulse amplitude V_D due to a bootstrap capacitance 51 between the points A and B (although this capacitance may be the parasitic capacitance of the MOST described previously, a capacitive element such as capacitor may alternatively be added externally, (and this applies to the various embodiments of this invention to be stated below), and the MOST T_1 operates in the non-saturation region of its characteristic. Hence, the pulse O_1 having the same waveform as that of the synchronizing pulse H_2 is provided at the point B. At this time, a MOST T_2 turns "on" simultaneously, and hence, "H" is applied to a point C. This potential becomes substantially equal to a value obtained by subtracting the threshold voltage of the MOST T_2 from the pulse amplitude V_D.

When the pulse H_1 subsequently becomes "H", MOSTs T_3 and T_4 turn "on", and "H" is applied to a point E for the same reason as before.

Further, when the pulse H_2 subsequently becomes "H", the pulse O_2 is similarly provided at a point F. At the time, also the MOST T_2 turns "on". Since "H" has been applied to the point C, charges stored therein flow back to the point B, the points B and C tend to have equal potentials, and the potential of the point B rises from zero towards a positive value.

In, for example, the solid-state imager, as regards horizontal output pulses, unless the pulse appears only once and the zero potential is maintained thereafter as depicted in Figure 5B, noise will increase. A MOST T_7 is a transistor for clearing the potentials of the point B and C to zero. Since the point F lying at the high level is connected to the gate electrode of MOST T_7, the MOST T_7 turns "on", and the points B and C are held fixed at the zero potential. A transistor T_8 has the same function as that of the transistor T_7, and clears points E and D to the zero potential.

The basic circuit of the scanning pulse generator circuit in Figure 5A is constructed of three MOSTs (for example, MOSTs T_3, T_4 and T_8),

and the points for deriving the output pulses are B, D, F. In Figure 5A, the output is thus derived every second stage, and discrete pulses synchronized with the clock pulses H_2 are obtained as shown by the output pulses O_1, O_2, O_3 in Figure 2B.

In the circuit shown in Figure 5A, no D.C. current flows, so that the power dissipation is as low as in the case where CMOS components are used. In addition, all the elements may be N-channel MOSTs.

In the circuit shown in Figure 5A, resetting transistors 61 and 62 are connected to the output points B, D, F. Due to the operation of the reset transistors, the operation of the circuit becomes more reliable. Even when the reset transistors are incorporated, the pitch of the shift register is not adversely affected.

Figure 6 shows a modification of the embodiment shown in Figure 5A, and it differs in the method of executing feedback. In Figure 5A, the potential of the point F is fed back to the point C. Conversely, in Figure 6, the point B receives feedback from the point F via MOST T_8, but it may alternatively receive feedback from the point E without any hindrance to the principle of the present invention.

Figure 7 shows a second embodiment of the present invention. The embodiment of Figure 7 is such that, in Figure 5A, the drain electrode of the transfer MOST T_2 is connected to the line of the power supply V_D, the output O_1 being applied to the gate of the MOST T_2. In the embodiment of Figure 5A, each time the synchronizing pulses H_1 and H_2 turn "on", the MOSTs T_2 and T_4 turn "on", and the charges of the points B and C move to gate electrodes. When the pulses H_1 and H_2 turn "off", some of the charges may escape to the substrate and the potential of the point C would then shift towards a positive value to some extent. The embodiment of Figure 7 avoids this disadvantage. The operating principle is substantially the same as in the embodiment of Figure 5A.

Even when the MOSTs T_1 and T_3 already have varactor capacitances consisting of parasitic capacitances, an additional capacitor can be provided to form a bootstrap capacitance.

Although the gate electrode of the feedback transistor T_6 in Figure 7 is connected to the point E, the feedback may alternatively be made from the point D.

It is also possible to locate reset transistors (not shown) at the output points (B, D, F) as in Figure 5A.

Figure 8 shows a third embodiment of the present invention. This embodiment is such that, compared to the circuit shown in Figure 5A, the feedback transistor T_7 is connected to the point B, not the point C.

In the foregoing first to third embodiments, the outputs O_1, O_2 and O_3 are the pulses which are synchronized with only one of the synchronizing pulse H_1 and H_2. However, this is not restricted to the case of using the embodiments as ordinary scanning circuits. For example, in Figures 5A and 5B, when the pulses H_1 and H_2 are pulses of an identical shape, output pulses are obtained from the points B, D and F. Thus this method of use is applicable to all the embodiments of the present invention.

A fourth embodiment of the present invention will now be discussed.

Figures 9A and 9B show the fourth embodiment of the scanning circuit of this invention and pulse waveforms of that circuit, respectively. A unit circuit is constructed from four MOSTs, for example, MOSTs T_{11}, T_{12}, T_{13} and T_{14}. Figure 9B is a waveform diagram of an input ϕ_{in}, driving pulses ϕ_1 and ϕ_2, and potentials at points 15A and 15B typical of the points in Figure 9A and at points 15C, 15F and 15I at which scanning pulses are obtained. Potentials similar to those of the points 15A and 15B appear as the potentials of points 15D and 14E and points 15G and 14H, with phase delays of 360° and 720° respectively. A terminal V_s is earthed, but even when it is coupled to the pulse ϕ_1 a similar effect is achieved (though the potential waveform of the point 15A changes to some extent).

The maximum potential which the point 15A attains is lowered by a ΔV_1 due to the threshold voltage V_{th} of the MOST T_{11} and the substrate effect, and further lowered by ΔV_2 due to the charging of the gate capacitance of the MOST T_{13}, whereupon the lowered potential is transferred to the node 15B to render the MOST T_{13} conductive. The potential of the point 15B is increased by the varactor-like effect (represented by a capacitance 151) due to the pulse ϕ_1, and rises by ΔV_s. If $\Delta V_s \geq V_{th} + \Delta V_1 + \Delta V_2$, the pulse ϕ_1 passes through the MOST T_{13} without any change (with the MOST T_{13} being in the non-saturation condition), and it is transferred to the output end, for example, the node 15C.

Owing to the gate electrode capacitance effect of the MOST T_{12}, a potential ΔV_4 appears at the points 15A and 15B each time the pulse ϕ_2 becomes positive as illustrated in Figure 9B, and it periodically renders the MOST T_{13} conductive. At this time, the pulse ϕ_1 is at earth potential, to execute the reset operation of stabilizing the output to the earth potential at all times. When only the threshold voltage of the MOST T_{14} is made higher than those of the other MOSTs, this effect is improved.

The scanning circuit of the present embodiment obtains the output pulses only from the driving pulse ϕ_1. In addition, it is not affected by deviations in the characteristics of the respective MOSTs, particularly the threshold voltages of the MOSTs T_{13}, etc., it is free from decay, so that the uniformity of operation is improved. Moreover, the required power is conspicuously low, and it is not necessary that the driver MOST should be disproportionately large relative to the load as is otherwise required for the inverter circuit, so that the embodiment is suited to a high degree of integration.

In order to more intensify the reset operation in the scanning circuit of Figure 9A, a MOST T_{15}

which connects the ϕ_1 line and the output by the use of pulse ϕ_1 may be situated in parallel with the MOST T_{13}. Even when the drain of the MOST T_{16} is connected to the earthed terminal V_S instead of the ϕ_1 line, a similar effect is achieved.

When a MOST T_{15} whose source and drain electrodes are connected to the ϕ_2 line and whose gate electrode is connected to the point between the MOSTs T_{11} and T_{12} is added, it demonstrates a varactor-like effect similar to that of the MOST T_{13}, eliminates ΔV_2 to be lowered by the charging of the gate capacitance of the MOST T_{13} and simplifies the design conditions.

When the above two measures are combined, that is, the MOSTs T_{15} and T_{16} are provided, both the effects are attained simultaneously. By providing a capacitive element in parallel with the varactor-like capacitance 151 of the MOST T_{13} shown in Figure 9A, ΔV_3 can be made greater. This is equivalent to increasing the capacitance 23 in Figure 2B and Figure 3B. The same effect is achieved in any of the other embodiments of the present invention.

Figures 10A and 10B show a fifth embodiment of the scanning circuit according to the present invention. Four MOSTs, for example, MOSTs T_{21}, T_{22}, T_{23} and T_{24} constitute a unit circuit. A waveform diagram of an input pulse ϕ_{in}, driving pulses ϕ_1 and ϕ_2, and potentials at points 18A to 18H typical of the points in Figure 10A is shown in Figure 10B.

The maximum potential to which, for example, the point 18C attains, is lowered by ΔV_1 due to the threshold voltage V_{th} of the MOST T_{21} and the body effect and is lowered further by ΔV_2 due to the charging of the gate capacitance of the MOST T_{23}, whereupon the lowered potential is transferred to the point 18D to render the MOST T_{23} conductive. The potential of the point 18D is increased by the varactor-like effect on the basis of the pulse ϕ_1, and rises by ΔV_3. If $\Delta V_3 \geq V_{th} + \Delta V_1 + \Delta V_2$, the pulse ϕ_1 passes through the MOST T_{23} without any change (with the MOST T_{23} being in the non-saturation condition), and it is transferred to the output or the point 18E.

Due to the gate electrode capacitance effect of the MOST T_{23}, a potential ΔV_4 appears at the points 18C and 18D each time the pulse ϕ_2 becomes positive as illustrated in Figure 10B, and it periodically renders the MOST T_{23} conductive. At this time, the pulse ϕ_1 is at earth potential, to execute the reset operation of stabilizing the output end to the earth potential at all times. When only the threshold voltage of the MOST T_{24} is made higher than those of the other MOSTs, this effect is improved.

In order to intensify the reset operation in the scanning circuit of Figure 10A, a MOST T_{25} which connects the ϕ_1 line and the output by the use of the pulse ϕ_2 can be provided in parallel with the MOST T_{23}. Even when the drain electrode of the MOST T_{25} is connected to earth instead of to the ϕ_1 line, a similar effect is achieved.

Further, when a MOST T_{26} whose source and drain electrodes are connected to the ϕ_2 line and whose gate electrode is connected to the point between the MOSTs T_{21} and T_{22} is added to the scanning circuit of Figure 10A, it demonstrates a varactor-like effect similar to that of the MOST T_{23}, eliminates ΔV_2 to be lowered by the charging of the gate capacitance of the MOST T_{23} and relieves restrictions on the design of the circuit.

Of course, when the above two measures are combined, that is, the MOSTs T_{25} and T_{26} are provided, both the effects are achieved simultaneously. By providing an additional capacitance in parallel with the varactor-like capacitance of the MOST T_{23} shown in Figure 10A, ΔV_3 can be made greater. This is equivalent to increasing the capacitance 23 in Figure 2B and Figure 3B. The same effect is achieved in any of the other embodiments.

Figure 11A shows a sixth embodiment of the scanning circuit according to the present invention. Figure 11B shows voltage waveforms at various points of the circuit shown in Figure 11A. The operation of this scanning circuit will now be briefly described. In the circuit of Figure 11A, when an input pulse ϕ_{IN} is applied, a MOST T_{31} is turned "on" by a clock pulse ϕ_2, and charges are stored in a lead 21Z (lead to the gate of a MOST T_{32}). Subsequently, when a synchronizing pulse ϕ_1 reaches a high level ("H"), a point 21A becomes "H", and also a MOST T_{33} turns "on" to make a point 21B "H". When the synchronizing pulse ϕ_1 falls to a low level (hereinafter abbreviated to "L"), the potential of the point 21A becomes "L", but the point 21B remains at "H" owing to the diode characteristic of the MOST T_{33}. The potential of the point 21B is the same as the potential of the gate electrode of a MOST T_{35}. When the synchronizing pulse ϕ_2 becomes "H", also points 21C and 21D become "H". When the synchronizing pulse ϕ_2 becomes "L" again, the potential of the point 21C becomes "L", whereas the potential of the point 21D remains at "H". Voltages are similarly transmitted to points 21E, 21F, 21G and 21H. When the potential of the point 21F becomes "H", the gate electrode of a MOST T_{34} becomes "H" and this MOST changes to the "on" state, and the potential of the point 21B is reset to V_{SS} or "L".

As seen from Figure 11B, a train of narrow pulses 21A, 21C, 21E, 21G, (spaced pulses) and a train of broad pulses 21B, 21D, 21F, 21H can be obtained as the outputs of the scanning circuit. the pulse amplitude of the pulses 21A, 21C, 21E, 21G, is the same as the pulse amplitude of the pulse ϕ_1 (or ϕ_2) owing to the bootstrap effect based on the gate to channel capacitances of the MOSTs T_{32}, T_{35}, T_{38}.

The power dissipation takes place only in the stage to which the input pulse is transmitted, and it is only necessary to charge the load, so that the power dissipation becomes very low.

As apparent from the above description, the scanning pulse generator circuit of the present embodiment consists of three MOSTs per stage. For example, the MOSTs T_{32}, T_{33} and T_{34} consistute one stage; and the drain electrode of

the MOST T_{32} serves as a synchonizing pulse-applying terminal, the gate electrode of the MOST T_{32} as an input terminal of the basis circuit, the node 21A as a scanning pulse output terminal, the point 21B as an output terminal of the basic circuit (it may also serve as the scanning pulse output terminal), the gate electrode of the MOST T_{34} as a feedback input terminal, and the source electrode of the MOST T_{34} as an earth terminal.

A modification of this embodiment is shown in Figure 12. This modification is such that, in order to intensify the bootstrap effects of the MOSTs T_{32}, T_{35}, T_{38} and T_{41} in Figure 11A, additional capacitances 221 are provided between the gate and source electrodes.

Figure 13 shows a second modification, in which in order to reset the potentials of the points 21B, 21D, to "L", signals are fed back from the points 21E, 21G to the gates of the MOSTs T_{34}, T_{37} (the modification differs from the embodiment of Figure 11A only in the place of feedback).

Figure 14 shows a third modification, in which additional capacitances 241 for intensifying the bootstrap effects are provided between the gates and sources of the MOSTs T_{32}, T_{35} in the embodiment of Figure 13.

Figure 15 shows a fourth modification. The sources of the resetting transistors T_{34}, T_{37}, T_{40} are connected to the ϕ_1 and ϕ_2 lines.

Figure 16 shows another example, in which additional capacitances 261 for intensifying the bootstrap effects are provided in the circuit arrangement shown in Figure 15.

Figure 17 shows another example. MOS varactors 271 are added to the embodiment of Figure 11A. As shown MOS reactors 271 are connected across the first and gate terminals of the first MISTs T_{32}, T_{35}, T_{38} etc of respective stages in the chain. The MOS reactors 271 have the property that the capacitances are large only when the gates are at "H". By way of example, if the potential of the point 21B is "H", the gate of the MOST T_{35} becomes sufficiently "H" due to the capacitance 271, and if the potential is "L", the capacitance 271 is small and has no disadvantageous effect. The MOS varactors can also be added to the examples shown in Figures 12 to 16.

Figure 18 shows a further modification. In order to improve the "L" potentials of the points 21A, 21C, 21E, 21G of the scanning circuit in Figure 13, MOSTs T_{51}, T_{52}, T_{53}, T_{54}, are added. These MOSTs for improved resetting can also be added to the examples of Figure 11A, Figure 12, and Figures 14 to 17.

Waveform diagrams for the circuits of Figures 12 to 18 are the same as those shown in Figure 11B.

Advantages of the embodiments described above are summarized below.

(a) Three MOSTs per stage suffice for most embodiments and the density of integration is enhanced. (However, four MOSTs per stage are required in the embodiment of Figure 18).

(b) With six MOSTs per stage, output pulses synchronized with only ϕ_1 (or ϕ_2) are obtained, and the non-uniformity of the output pulses is reduced.

(c) When the nodes 21A, 21C, 21E, 21G are employed as output terminals, the amplification of the output pulses is the same as that of $\phi 1$ (or $\phi 2$), the V_{TH} drop due to MOSTs does not occur.

(d) When considering the output pulse widths, a pulse equal to the synchronizing pulse width (narrow pulse width) and a pulse equal to the synchronizing pulse period (broad pulse width) are obtained.

(e) Inferior parasitic effects (charge pumping etc.) do not occur when integrated circuits are used.

(f) The power dissipation is very low.

(g) In order to operate the scanning circuit, only ϕ_1, ϕ_2, ϕ_{IN} and V_{SS}(GND) are required, and V_{DD} is unnecessary.

Figure 19A shows a terminating circuit of the above scanning circuits, while Figure 19B shows synchronizing pulses, an input pulse and potential variations at various nodes.

The circuit is such that MOSTs T_{61}, T_{62}, T_{63}, T_{64} and T_{65} are connected to the embodiment of Figure 11A.

The potential of a point 21F is reset only when the potential of a point 21H is "H", and is reset by a pulse 21I synchronized with ϕ_1 by the MOST T_{61}. The potential of a point 21H is reset only when the potential of a point 21G is "L", and is reset by a pulse 21J synchronized with ϕ_2 by the MOST T_{63}. The g_m ratio between the MOSTs T_{63} and T_{64} may be set approximately to $g_{m.64}/g_{m.63} = 8$. The MOST T_{62} need not be provided, but it may be incorporated in order to make the operation more reliable.

Although the line V_s is shown as earthed in Figures 5A and 6 only, the line V_s may be earthed in each of the other embodiments or may, in all cases be at some other suitable reference voltage.

CLAIMS

1. A circuit for generating scanning pulses comprising a plurality of stages of basic circuits connected in series, each basic circuit including a first and second and a third insulated gate field-effect transistors (hereinafter referred to as MISTs), each MIST having a first and a second terminal and a gate terminal;

the first terminal of said first MIST being used as a synchronizing-pulse-applying terminal, the second terminal of said first MIST being used as a scanning pulse output terminal, and the gate terminal of said first MIST being used as an input terminal;

the first terminal and the gate terminal of said second MIST being electrically connected together and to the second terminal of said first MIST, and the second terminal of said second MIST being used as an output terminal;

the first terminal of said third MIST being electrically connected to the second terminal of said second MIST, the second terminal of said third MIST being used as an earth terminal, and the gate terminal of said third MIST being used

as a feedback input terminal.

2. A circuit for generating scanning pulses according to claim 1, wherein said feedback input terminal of a first basic circuit is connected to the output terminal of a second basic circuit which is two stages ahead of the first basic circuit in the series of basic circuits.

3. A circuit for generating scanning pulses according to claim 1, wherein said feedback input terminal of a first basic circuit is connected to the scanning pulse output terminal of a second basic circuit which is two stages ahead of the first basic circuit in the series of basic circuits.

4. A circuit for generating scanning pulses according to any one of the preceding claims, wherein the earth terminals of the basic circuits of odd stages have the second synchronizing pulse applied thereto, and the earth terminals of the basic circuits of even stages have the first synchronizing pulse applied thereto.

5. A circuit for generating scanning pulses according to any one of the preceding claims, further comprising a plurality of MOS varactors the MOST reactors being connected across the first and gate terminals of the first MISTs of respective stages in the chain.

6. A circuit for generating scanning pulses comprising a plurality of stages of basic circuits connected in series, each basic circuit including a first a second and a third insulated gate field-effect transistors (hereinafter referred to as MISTs), each MIST having a first and a second terminal and a gate terminal;

the first terminal of said first MIST being used as a synchronizing-pulse-applying terminal, the second terminal of said first MIST being used as a scanning pulse output terminal, and the gate terminal of said first MIST being used as an input terminal;

the first terminal of said second MIST being electrically connected to the second terminal of said first MIST, the second terminal of said second MIST being used as an output terminal, and the gate terminal of said second MIST being connected to the synchronizing-pulse-applying terminal;

the first terminal of said third MIST being electrically connected to either the scanning pulse output terminal or the output terminal, the second terminal of the third MIST being used as earth terminal, and the gate terminal of said third MIST being used as a feedback input terminal.

7. A circuit for generating scanning pulses according to claim 6, wherein a first terminal of a fourth MIST whose gate has a synchronizing pulse applied thereto is connected to said output terminal of said basic circuit, and a second terminal of said fourth MIST is connected to the input terminal of the basic circuit of the succeeding stage.

8. A circuit for generating scanning pulses according to claim 7, wherein said feedback input terminal of a first basic circuit is connected to the output terminal of the basic circuit of a succeeding stage.

9. A circuit for generating scanning pulses according to claim 8, wherein said earth terminal is connected to said scanning pulse output terminal.

10. A circuit for generating scanning pulses comprising a plurality of stages of basic circuits connected in series, each basic circuit including a first a second and a third insulating gate field-effect transistors (hereinafter referred to as MISTs), each MIST having a first and a second terminal and a gate terminal;

the first terminal of said first MIST being used as synchronizing-pulse-applying terminal, and second terminal of said first MIST being used as a scanning pulse output terminal, and

the gate terminal of said first MIST being used as an input terminal;

the first terminal of said second MIST being used as a power supply terminal, the second terminal of said second MIST being used as an output terminal, and the gate terminal of said second MIST being electrically connected to the second terminal of said first MIST;

the first terminal of said third MIST being electrically connected to either the scanning pulse output terminal or the output terminal, the second terminal of said third MIST being used as an earth terminal, and the gate terminal of said third MIST being used as a feedback input terminal.

11. A circuit for generating scanning pulses according to claim 10, wherein the power supply terminals of respective basic circuits are connected to a common power supply line.

12. A circuit for generating scanning pulses according to any one of claim 6, 10 or 11, wherein said feedback input terminal of a first basic circuit is connected to either the scanning pulse output terminal or the output terminal of a second basic circuit which is two stages ahead of a first basic circuit in the series of basic circuits.

13. A circuit for generating scanning pulses according to any one of the preceding claims, wherein the synchronizing pulse-applying terminals of the basic circuits of odd stages have a first sycnhronizing pulse applied thereto, and the synchronizing pulse-applying terminals of the basic circuits of even stages have a second synchronizing pulse applied thereto.

14. A circuit for generating scanning pulses according to any one of the preceding claims, wherein said first MIST has a bootstrap capacitance between said gate terminal and said second terminal, said bootstrap capacitance consisting of parasitic capacitances.

15. A circuit for generating scanning pulses as according to any one of the preceding claim, wherein said first MIST has a capacitor connected between its gate terminal and second terminal.

16. A circuit for generating scanning pulses according to any one of the preceding claims, wherein the earth terminals of the respective basic circuits are connected to a common earth line.

17. A circuit for generating scanning pulses according to any one of the preceding claims, further comprising a fifth MIST whose drain is

connected to said scanning pulse output terminal, whose source is connected to an earth line and whose gate has a synchronizing pulse applied thereto.

18. A circuit for generating scanning pulses according to any one of the preceding claims, wherein scanning pulses are obtained from the scanning pulse output terminals of the basic circuits of every alternate stage.

19. A circuit for generating scanning pulses according to any one of the preceding claims, further comprising an input MIST, a first terminal of said input MIST being used as an input pulse-applying terminal, a second terminal of said input MIST being connected to the input terminal of the basic circuit of the first stage, a gate terminal of said input MIST being used as a synchronizing pulse-applying terminal.

20. A circuit for generating scanning pulses substantially as herein described with reference to, and as illustrated in Figure 5A, Figure 6, Figure 7, Figure 8, Figure 9A, Figure 10A, Figure 11A, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17 or Figure 18 or Figures 11A and 19A of the accompanying drawings.

New claims or amendments to claims filed on 18th September 1979.

Superseded claims 5 and 15.

New or amended claims:—

5. A circuit for generating scanning pulses according to any one of the preceding claims, further comprising a plurality of MOS varactors (variable capacitors or varicaps), the MOS varactors being connected across the first and gate terminals of the first MISTs of respective stages in the chain.

15. A circuit for generating scanning pulses as according to any one of the preceding claims, wherein said first MIST has an additional capacitor connected between its gate terminal and second terminal.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1979. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.